WHAT IS CLAIMED IS:

1. A method of forming a ferroelectric memory device, comprising:

preparing a semiconductor substrate comprising an interlayer dielectric layer and a capacitor lower electrode contact formed through the interlayer dielectric layer;

forming a cylindrical capacitor lower electrode on the interlayer dielectric layer, thereby covering the contact;

conformally stacking a ferroelectric layer by using a chemical vapor deposition (CVD) technique over substantially the entire surface of the semiconductor substrate including the capacitor lower electrode; and

forming a capacitor upper electrode in the shape of a spacer surrounding the sidewall of the ferroelectric layer.

2. The method as claimed in claim 1, further comprising forming a plate line over a region of the semiconductor substrate where the upper electrode is formed, the plate line being in electrical contact with the upper electrode.

3. The method as claimed in claim 2 in which plural ones of such capacitors are arranged across the semiconductor substrate surface, after forming the upper electrode and before forming the plate line, further comprising:

stacking an insulation layer over substantially the entire surface of the semiconductor substrate, to partially fill gaps between the capacitors,

the insulation layer exposing at least a part of the upper electrode.

4. The method as claimed in claim 3, wherein:

the recessing of the insulation layer is performed by an etching process; and

the etching process uses an etch gas including at least one gas selected from a group consisting of CHF3, CF4, Ar, and N2 to make the insulation layer have etch selectivities with respect to the upper electrode and the ferroelectric layer.

5. The method as claimed in claim 1, wherein the forming of the lower electrode further comprises:

sequentially stacking a lower electrode layer and a hard mask layer over substantially the entire surface of the semiconductor substrate;

forming a hard mask pattern through photolithography and etching processes with respect to the hard mask layer; and

etching the lower electrode layer by using the hard mask pattern as an etch mask to form the lower electrode.

6. The method as claimed in claim 5, further comprising;

stacking a conductive adhesive assistant layer before stacking the lower electrode layer, wherein the adhesive assistant layer is patterned together with the lower electrode layer.

7. The method as claimed in claim 1, wherein the forming of the lower electrode comprises:

forming a sacrificial layer at the semiconductor substrate;

forming a contact hole at the lower electrode region of the sacrificial layer;

filling the contact hole with a conductive layer; and

removing a remnant part of the sacrificial layer.

8. The method as claimed in claim 7, wherein the filling of the contact hole is performed by an electroplate technique.

9. The method as claimed in claim 1, wherein:

the forming of the upper electrode further comprises stacking an upper electrode layer at the entire surface of the semiconductor substrate and anisotropically etching the entire surface of the upper electrode to expose the ferroelectric layer; and

the anisotropical etching of the upper electrode layer uses an etch gas including oxygen and a combination gas composed of at least one gas selected from a group consisting of Cl2, BCl3, HBr, and Ar, to make the upper electrode layer have an etch selectivity with respect to the ferroelectric layer.